EE/CPRE/SE 491 - sddec24-13

ReRAM Compute ASIC Fabrication

Weekly Report 9

4/2/24 - 4/9/24

Client: Prof. Henry Duwe

Advisor: Prof. Cheng Wang

Team Members:

- Gage Moorman - Team Organizer, main analog designer
- Konnor Kivimagi - Main documentation editor, mixed analog digital designer
- Nathan Cook – Main client liaison, mixed analog digital designer
- Jason Xie – Assistant documentation editor, main digital designer

Weekly summary:

This week, we solved the ReRAM model issue and proved it simulated. We also began sizing the TIA as well as simulating and testing the ADC.

Past Week Accomplishments:

- Fixed ReRAM model
    - It is now able to be simulated
- Simulated first stages of ADC
- Top level of logic analyzer is finished
    - Still have to write verilog but should have function already written and planned out

Individual Contributions:

Team Member	Contributions	Weekly hours	Total Hours
Konnor Kivimagi	Solved ReRAM model issue.	5	61
Gage Moorman	began simulating and Testing ADC. Helped with TIA sizing and simulations	6	60
Nathan Cook	Got some work done on controller design, mostly top level.	5	57
Jason Xie	Developed and tested a priority encoder. Working on inserting digital circuits into Xschem. Continued sizing TIA devices.	6	58

Pending Issues:

- No straightforward way to analyze xschem/ngspice data on outside applications
- Need to update website
- Do not know how to synthesize Verilog in xschem for ADC or logic analyzer
- Having difficulty using ngspice and xschem analysis tools effectively
- Having capacitance issues on bit 8 node of ADC

Plans for the coming week:

- Gage Moorman
    - Finalize Sizing of Comparator Transistors
    - Create resistor ladder for ADC and Encoder Verilog
    - Simulate and test full ADC design
    - Build upon analog documentation
- Konnor Kivimagi
    - Run simulations on ReRAM model
    - Start preparing for final presentation
- Nathan Cook
    - Get verilog written for logic analyzer
        - May test in modelsim then transfer over to open-source tools
    - Update website
- Jason Xie
    - Find a way to implement digital components in Xschem design space
    - Finish sizing and testing TIA

Summary of Advisor Meeting:

We had a brief meeting this week where we discussed conveying in more detail what each member was doing each week. We also discussed that our documentation could be organized into one folder to make it more accessible to everyone and a weekly progress update in presentation form.